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1 Single-Track Asynchronous Pipeline Templates Using 1-of-N Encoding

M. Ferretti, P. Beerel

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(163.22 KB) Publisher Site Additional Information: full citation, abstract

This paper presents a new fast and templatizedfamily of fine-grain asynchronous pipeline stages basedon the single-track protocol. No explicit control wiresare required outside of the datapath and the data is 1-of-N encoded. With a forward latency of 2 transitionsand a cycle time of 6 for most configurations, the newfamily can run at 1.6 GHz using MOSIS TSMC 0.25 µmprocess. This is significantly faster than all knownquasi-delay-insensitive templates and has less timingassumptions than the recent ...

2 FPGA routing architecture: segmentation and buffering to optimize speed and density

Vaughn Betz, Jonathan Rose

February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays**

Full text available: pdf(1.36 MB) Additional Information: full citation, references, citings, index terms

3 Efficient circuit clustering for area and power reduction in FPGAs

Amit Singh, Ganapathy Parthasarathy, Malgorzata Marek-Sadowska

October 2002 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 7 Issue 4

Full text available: pdf(3.26 MB) Additional Information: full citation, abstract, references, index terms

We utilize Rent's rule as an empirical measure for efficient clustering and placement of circuits in clustered Field Programmable Gate Arrays (FPGAs). We show that careful matching of resource availability and design complexity during the clustering and placement processes can contribute to spatial uniformity in the placed design, leading to overall device decongestion after routing. We present experimental results to show that appropriate logic depopulation during clustering can have a positive ...

Keywords: FPGA, Rent, clustering, congestion, interconnect, placement, power

4 A detailed power model for field-programmable gate arrays

Kara K. W. Poon, Steven J. E. Wilton, Andy Yan
April 2005 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 10 Issue 2
Full text available: pdf(822.20 KB) Additional Information: full citation, abstract, references, index terms

Power has become a critical issue for field-programmable gate array (FPGA) vendors. Understanding the power dissipation within FPGAs is the first step in developing power-efficient architectures and computer-aided design (CAD) tools for FPGAs. This article describes a detailed and flexible power model which has been integrated in the widely used Versatile Place and Route (VPR) CAD tool. This power model estimates the dynamic, short-circuit, and leakage power consumed by FPGAs. It is the first fl ...

Keywords: Power estimation model, architecture, power consumption, sensitivity analysis

5 Physical Design: Efficient circuit clustering for area and power reduction in FPGAs
Amit Singh, Malgorzata Marek-Sadowska
February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**
Full text available: pdf(935.90 KB) Additional Information: full citation, abstract, references, citings

We present a routability-driven bottom-up clustering technique for area and power reduction in clustered FPGAs. This technique uses a cell connectivity metric to identify seeds for efficient clustering. Effective seed selection, coupled with an interconnect-resource aware clustering and placement, can have a favorable impact on circuit routability. It leads to better device utilization, savings in area, and reduction in power consumption. Routing area reduction of 35% is achieved over previously ...

6 Energy aware design: Optimizing pipelines for power and performance
Viji Srinivasan, David Brooks, Michael Gschwind, Pradip Bose, Victor Zyuban, Philip N. Strenski, Philip G. Emma
November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**
Full text available: pdf(1.24 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

During the concept phase and definition of next generation high-end processors, power and performance will need to be weighted appropriately to deliver competitive cost/performance. It is not enough to adopt a CPI-centric view alone in early-stage definition studies. One of the fundamental issues confronting the architect at this stage is the choice of pipeline depth and target frequency. In this paper we present an optimization methodology that starts with an analytical power-performance model ...

7 A power estimation model for high-speed CMOS A/D converters
E. Lauwers, G. Gielen
January 1999 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(50.46 KB) Additional Information: full citation, citings, index terms

8 Towards a better understanding of failure modes and test requirements of ADCs
A. Lechner, A. Richardson, B. Hermes
March 2001 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(30.48 KB) Additional Information: full citation, references, index terms

9 Architecture Analysis and Automation: On the sensitivity of FPGA architectural conclusions to experimental assumptions, tools, and techniques
Andy Yan, Rebecca Cheng, Steven J. E. Wilton
February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**
Full text available: pdf(291.87 KB) Additional Information: full citation, abstract, references, citings

Recent years have seen a tremendous increase in the capacities and capabilities of Field-Programmable Gate Arrays (FPGA's). Much of this dramatic improvement has been the result of changes to the FPGAs' internal architectures. New architectural proposals are routinely generated in both academia and industry. For FPGA's to continue to grow, it is important that these new architectural ideas are fairly and accurately evaluated, so that those worthy ideas can be included in future chips. Typically, ...

10 Session 3C: Routing architecture and techniques for FPGAs: Interconnect resource-aware placement for hierarchical FPGAs
Amit Singh, Ganapathy Parthasarathy, Malgorzata Marek-Sadowska
November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(1.16 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we utilize Rent's rule as an empirical measure for efficient clustering and placement of circuits on hierarchical FPGAs. We show that careful matching of design complexity and architecture resources of hierarchical FPGAs can have a positive impact on the overall device area. We propose a circuit placement algorithm based on Rent's parameter and show that our clustering and placement techniques can improve the overall device routing area by as much as 21% for the same array size, w ...

11 Routing the 3-D chip
Richard J. Enbody, Gary Lynn, Kwee Heong Tan
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**
Full text available: pdf(504.68 KB) Additional Information: full citation, references, index terms

12 Using sparse crossbars within LUT
Guy Lemieux, David Lewis
February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**
Full text available: pdf(168.45 KB) Additional Information: full citation, abstract, references, citings, index terms

In FPGAs, the internal connections in a cluster of lookup tables (LUTs) are often fully-connected like a full crossbar. Such a high degree of connectivity makes routing easier, but has significant area overhead. This paper explores the use of sparse crossbars as a switch matrix inside the clusters between the cluster inputs and the LUT inputs. We have reduced the switch densities inside these matrices by 50% or more and saved from 10 to 18% in area with no degradation to critical-path delay ...

13 Magic's circuit extractor
Walter S Scott, John K. Ousterhout
June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**
Full text available: pdf(801.39 KB) Additional Information: full citation, abstract, references, citings, index terms

We have implemented a fast hierarchical circuit extractor for the Magic VLSI layout system.

The keys to its speed are a new algorithm based on corner-stitching, and its ability to extract cells incrementally. Because the extractor is incremental, typically only a few cells must be re-extracted when the layout changes. The extractor computes circuit connectivity and transistor dimensions, both internodal and substrate parasitic capacitance, and parasitic resistances. It is p ...

14 Power minimization in IC design: principles and applications

Massoud Pedram

January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1

Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

15 Automatic layout algorithms for function blocks of CMOS gate arrays

Shigeo Noda, Hitoshi Yoshizawa, Etsuko Fukuda, Haruo Kato, Hiroshi Kawanishi, Takashi Fujii

June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**

Full text available: pdf(620.96 KB) Additional Information: full citation, abstract, references, citings, index terms

Automatic layout algorithms, placement and routing, for function blocks of CMOS gate arrays are presented. The placement algorithm assigns transistors to basic cells so as to minimize the number of cells used and to minimize the number of interconnections crossing cut-lines. The former objective is achieved by finding a maximum matching and the latter is achieved by iterative interchanges of transistor pairs. A new routing technique based on channel routing methods is introduced ...

16 A statistical response surface generator

James Roger Corliss

January 1974 **Proceedings of the 7th conference on Winter simulation - Volume 2**

Full text available: pdf(328.89 KB) Additional Information: full citation, abstract, index terms

Small scale special purpose analog simulators are finding many applications as teaching aids in the classroom. One type of simulator design is currently being used in graduate level statistics courses at the University of Delaware. It was developed primarily for teaching Statistical Response Surface Technology. Statistical Response Surface Technology (SRST) is an effective way of optimizing variables in a system or process. Samples at various operating parameters are taken and an ...

17 Transistor placement for noncomplementary digital VLSI cell synthesis

Michael A. Riepe, Karem A. Sakallah

January 2003 **ACM Transactions on Design Automation of Electronic Systems**

(TODAES), Volume 8 Issue 1
Full text available: pdf(2.97 MB) Additional Information: full citation, abstract, references, index terms

There is an increasing need in modern VLSI designs for circuits implemented in high-performance logic families such as Cascode Voltage Switch Logic (CVSL), Pass Transistor Logic (PTL), and domino CMOS. Circuits designed in these noncomplementary ratioed logic families can be highly irregular, with complex diffusion sharing and nontrivial routing. Traditional digital cell layout synthesis tools derived from the highly stylized "functional cell" style break down when confronted with such circuit t ...

Keywords: Cell Synthesis, Euler graphs, benchmark circuits, digital circuits, noncomplementary circuits, sequence pair optimization, transistor chaining, transistor placement

18 A novel methodology for transistor-level power estimation
S. Huang, K. Cheng, K. Chen, T. Lee
August 1996 **Proceedings of the 1996 international symposium on Low power electronics and design**
Full text available: pdf(221.08 KB) Additional Information: full citation, references, citings, index terms

19 New directions in traffic measurement and accounting: Focusing on the elephants, ignoring the mice
Cristian Estan, George Varghese
August 2003 **ACM Transactions on Computer Systems (TOCS)**, Volume 21 Issue 3
Full text available: pdf(1.03 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Accurate network traffic measurement is required for accounting, bandwidth provisioning and detecting DoS attacks. These applications see the traffic as a collection of flows they need to measure. As link speeds and the number of flows increase, keeping a counter for each flow is too expensive (using SRAM) or slow (using DRAM). The current state-of-the-art methods (Cisco's sampled NetFlow), which count periodically sampled packets are slow, inaccurate and resource-intensive. Previous work showed ...

Keywords: Network traffic measurement, identifying large flows, on-line algorithms, scalability, usage based accounting

20 PALACE: a layout generator for SCVS logic blocks
Knut M. Just, Edgar Auer, Werner L. Schiele, Alexander Schwaferts
January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**
Full text available: pdf(856.11 KB) Additional Information: full citation, abstract, references, index terms

A novel approach to the automatic layout synthesis of dynamic CMOS circuits is presented. A set of logic expressions is realized in a row of cells. Taking multi-level Boolean expressions as input, logic transistors are placed and routed. Efficient solutions are achieved by permuting the variables of the expressions and by row folding. The layout is designed on a coarse grid taking timing requirements into account and afterwards adapted to the geometric design rules by a compactor. A compari ...